Electronic Version

Stylesheet Version v1.1.1

A Divide-by-X.5 Circuit with Frequency Doubler and Differential Oscillator

Abstract

A divide by X.5 circuit can be implemented as a divided by 1.5 circuit. A phase-locked loop (PLL) has a quadrature voltage-controlled oscillator (VCO) that generates four phases offset at 0, 90, 180, and 270 degrees. Differential signals from the VCO are converted to single-ended VCO clocks that drive four divide-by-3 circuits, each clocked by one of the four phases of the VCO clocks. Resets to the divide-by-3 circuits are staggered to activate each divide-by-3 circuit synchronously with its phase clock. Outputs from the divide-by-3 circuits are applied to a frequency doubler that generates the final clock that is 1.5 times slower than the VCO clocks. The final clock has a near 50%-50% duty cycle.